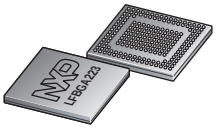


SAF360X

Digital radio and processing system-on-chip

Rev. 2 — 22 August 2014 Product short data sheet

1. General description

The SAF360X is a monolithic integrated digital terrestrial radio processor. The SAF360X family includes different chip variants—SAF3600, SAF3601, SAF3602, SAF3604, SAF3606, SAF3607. The SAF360X provides reception, demodulation, audio decoding and application processing for various digital radio standards.

The SAF360X system-on-chip (SoC) is a next generation HD Radio/DAB/DAB+/T-DMB/DRM solution for breakthrough in system cost reduction. The chip is qualified in accordance with AEC-Q100 and includes the following benefits:

- Next generation HD Radio / DAB / DAB+ / T-DMB / DRM solution for breakthrough in system cost reduction
- Dual channel processing with the on-chip dual DAB front-end, memory and source decoding
- End-of-production line programmability
- DAB-FM / DAB-DAB blending
- Advanced reception improvement algorithms
- Integrated antenna buffer enabling antenna diversity via an external transistor from 3.3 V (SAF3601, SAF3602, SAF3604, SAF3606 only)
- On chip voltage regulation for performance critical Front-end supply
- Single system XTAL with optional clock reference output capabilities
- Ultra small PCB footprint using state-of-the-art BGA package

2. Features and benefits

2.1 HD Radio technology

- HD Radio signal decoding for AM and FM digital audio
- HD Radio 1.5 support for background scanning and data services through the second tuner
- HD all-digital mode support
- SAF3604: On-chip FM-tuner for data service reception
- Dual baseband input interface using I^2S-bus derivative with I/Q
- Secondary baseband interface for dual tuner applications
- Meta data support for HD Radio reception
- Advanced HD Radio feature support (contact NXP Sales for a detailed list of supported feature sets; see Section 11)

- Apple ID3 tag
- Multicasting

- Electronic Program Guide (EPG)
- Off-chip LOT processing
- Reception improvement (Maximum Ratio Combining (MRC))

2.2 DRM

- DRM signal decoding for AM and FM digital audio
- Prepared for dual DRM support with background scanning or data services from second station
- Frontend to baseband interface through serial I^2S-bus type interface
- Prepared for secondary baseband interface for dual tuner applications
- Channel decoder reception improvements
- Prepared for DRM+

2.3 DAB, DAB+ and T-DMB radio technology

- SAF3601, SAF3602, SAF3606: Dual reception processing with on-chip dual DAB front-end, ADC, memory and source decoding
- Data service reception and filtering
- Full dual ensemble processing (2×1.8 Mbit/s)
- SAF3601, SAF3602, SAF3606: Optional third tuner input via serial I^2S-bus type interface
- Integrated DAB-FM/ DAB-DAB time alignment and seamless blending
- Integrated support for all actual audio codecs (AAC, HE-AAC, MP2, BSAC)
- (Optional) Additional features:
  - Reception improvement algorithms for single antenna systems delivering additionally improved BER
  - Diversity reception improvement through advanced Maximum Ratio Combining (MRC) algorithms leveraging dual antenna diversity
  - Third external tuner supports enabling background service scan or data services in case of two primary Saturn tuners are used for antenna diversity reception

2.4 Digital audio

- Up to 6 channel (5.1) audio support through TDM audio interface
- Programmable audio sample rate converter (8 kHz to 48 kHz) for up to 6 channels
- I^2S audio input for auxiliary processing
- Optional SRC (8 kHz to 48 kHz) for I^2S-bus input
- Optional support for input and output 96 kHz sample rate conversion
- Basic audio processing for external digital audio sources
- Advanced audio processing (contact NXP for a list of supported audio processing features; see Section 11)

2.5 Other peripheral interfaces

- Two I^2C-bus interfaces

- Two Serial Peripheral Interfaces (SPI)
- One High-Speed Serial Peripheral Interface (HS-SPI)
- One UART interface
- 16 individual GPIO pins for applications and diagnostics
- One JTAG interface for diagnostics

2.6 Additional features

- Secure boot, image authentication
- Identical radio architecture with the same chip and specific software for various standards including DAB, HD Radio and DRM
- Radio control reuse from SAF356X with same API
- In field software upgrade possibility using SPI and I^2C interface connections to external flash memories
- One internal clock oscillator and two internal Phase-Locked Loops (PLL)
- Powerful signal, audio processing core architecture
- Qualified in accordance with AEC-Q100

Remark: Not all features are available on all variants or in all combinations. Contact NXP sales for more information; see Section 11 “Contact information”.

3. Applications

- Application depends on usages and reception standard

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SAF3601, SAF3602, SAF3604, SAF3606							
$V_{DDA(VREG)(3V3)}$	voltage regulator analog supply voltage			3.0	3.3	3.6	V
$V_{DDA(ADPLL1)(1V8)}$	ADPLL1 analog supply voltage			1.71	1.8	1.89	V
$V_{DDA(XTAL)(1V8)}$	crystal analog supply voltage			1.71	1.8	1.89	V
$V_{DDA(DCO1)(1V8)}$	DCO1 analog supply voltage			1.58	1.8	1.89	V
$V_{DDA(DIV)(1V8)}$	DIV analog supply voltage			1.71	1.8	1.89	V
$V_{DDA(LVHFA)(1V8)}$	LVHFA analog supply voltage			1.71	1.8	1.89	V
$V_{DDA(VHFM)(1V8)}$	VHFM analog supply voltage			1.71	1.8	1.89	V
$V_{DDA(DCO2)(1V8)}$	DCO2 analog supply voltage			1.58	1.8	1.89	V
$V_{DDA(ADPLL2)(1V8)}$	ADPLL2 analog supply voltage			1.71	1.8	1.89	V
$V_{DDA(ADC)(1V8)}$	ADC analog supply voltage			1.71	1.8	1.89	V
$V_{DDD(ADPLL1)(1V8)}$	ADPLL1 digital supply voltage			1.71	1.8	1.89	V
$V_{DDD(ADPLL2)(1V8)}$	ADPLL2 digital supply voltage			1.71	1.8	1.89	V
$V_{DDD(RFE)(1V8)}$	RFE digital supply voltage			1.71	1.8	1.89	V
$V_{DD(IO)}$	input/output supply voltage			3.0	3.3	3.6	V
V_{QPS}	OTP programming voltage (2.5 V)			2.25	2.5	2.75	V

Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(A)}$	analog blocks supply voltage		1.14	1.2	1.26	V
$V_{DD(C)}$	core supply voltage		1.14	1.2	1.26	V
SAF3600, SAF3607						
$V_{DD(IO)}$	input/output supply voltage		3.0	3.3	3.6	V
V_{QPS}	OTP programming voltage (2.5 V)		2.25	2.5	2.75	V
$V_{DD(A)}$	analog blocks supply voltage		1.14	1.2	1.26	V
$V_{DD(C)}$	core supply voltage		1.14	1.2	1.26	V
P_{tot}	total power dissipation		-	0.46	0.61	W

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SAF36xxEL/Vyyyz	LFBGA223	plastic low profile fine-pitch ball grid array package; 223 balls	SOT1322-1

Table 3. Type overview

Not all variants are commercially released. Please contact NXP Sales for further details.

Type number	Main application	Clock
HD subtypes		
SAF3600EL/V1040	single external tuner (HD 1.0)	55.4667 MHz
SAF3600EL/V1041	single external tuner (HD 1.0)	10.4 MHz – 12.288 MHz
SAF3600EL/V1042	dual external tuner (HD 1.5)	55.4667 MHz
SAF3600EL/V1043	dual external tuner (HD 1.5)	10.4 MHz – 12.288 MHz
SAF3604EL/V3040	single internal tuner (HD 1.5)	55.4667 MHz
DAB subtypes		
SAF3601EL/V3040	single internal tuner (DAB 1.0)	55.1922 MHz, 55.4667 MHz
SAF3602EL/V3040	dual internal tuner (DAB 1.5)	55.1922 MHz, 55.4667 MHz
DRM subtypes		
SAF3607EL/V1040	single external tuner (DRM1.0)	55.4667 MHz
SAF3607EL/V1041	single external tuner (DRM1.0)	10.4 MHz – 12.288 MHz
Premium		
SAF3606EL/V3040	all standards (HD, DAB, DRM) customer configurable	55.1922 MHz, 55.4667 MHz

6. Block diagram

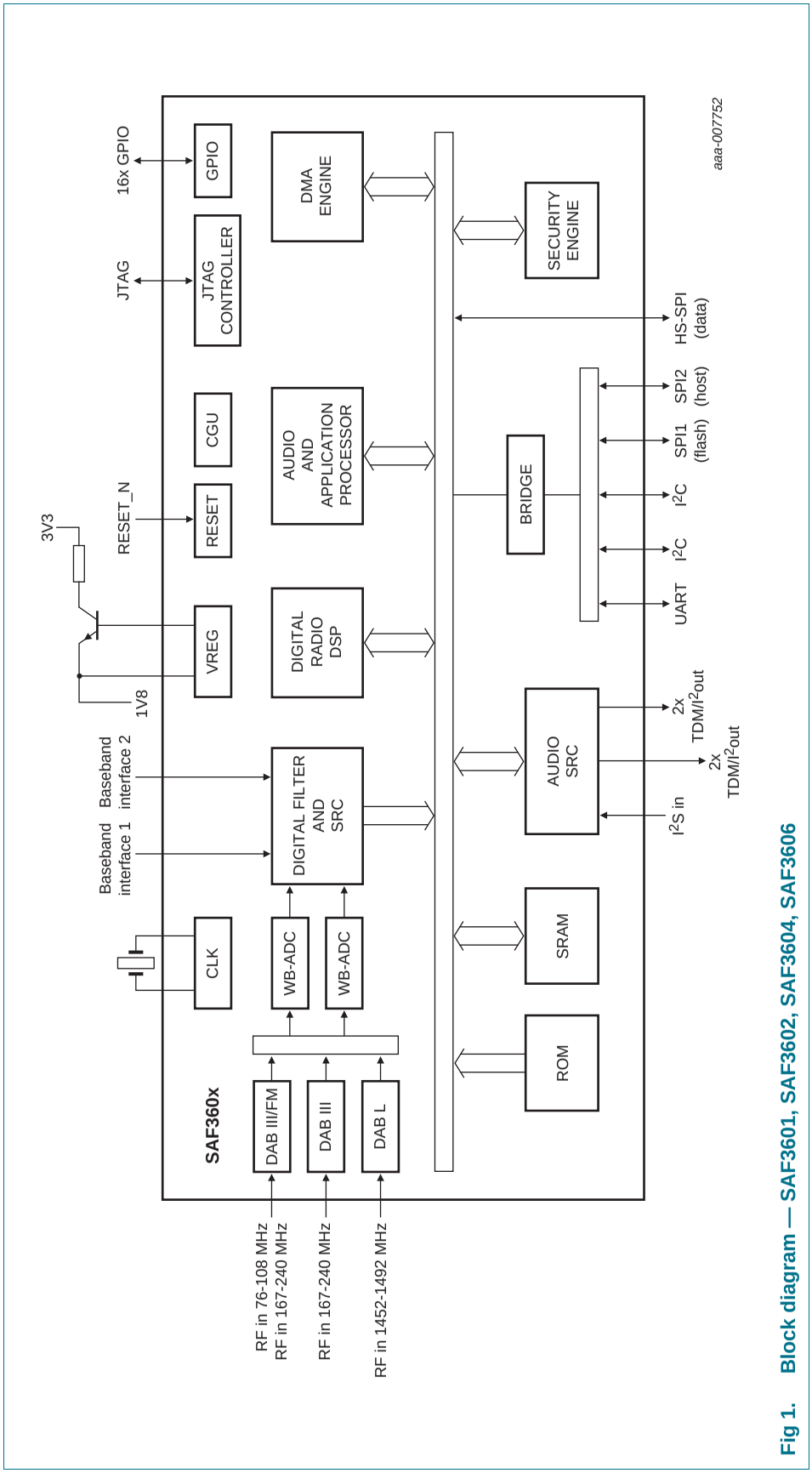


Fig 1. Block diagram — SAF3601, SAF3602, SAF3604, SAF3606

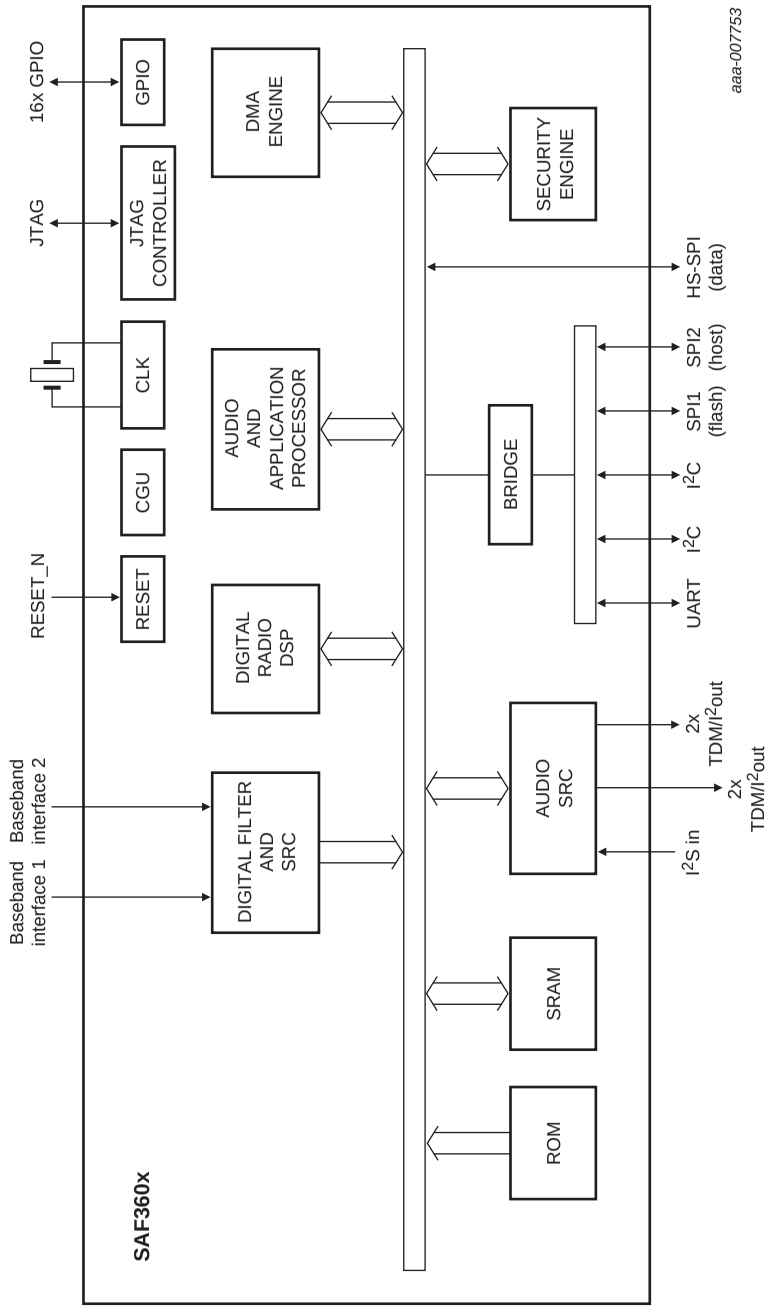


Fig 2. Block diagram – SAF3600, SAF3607

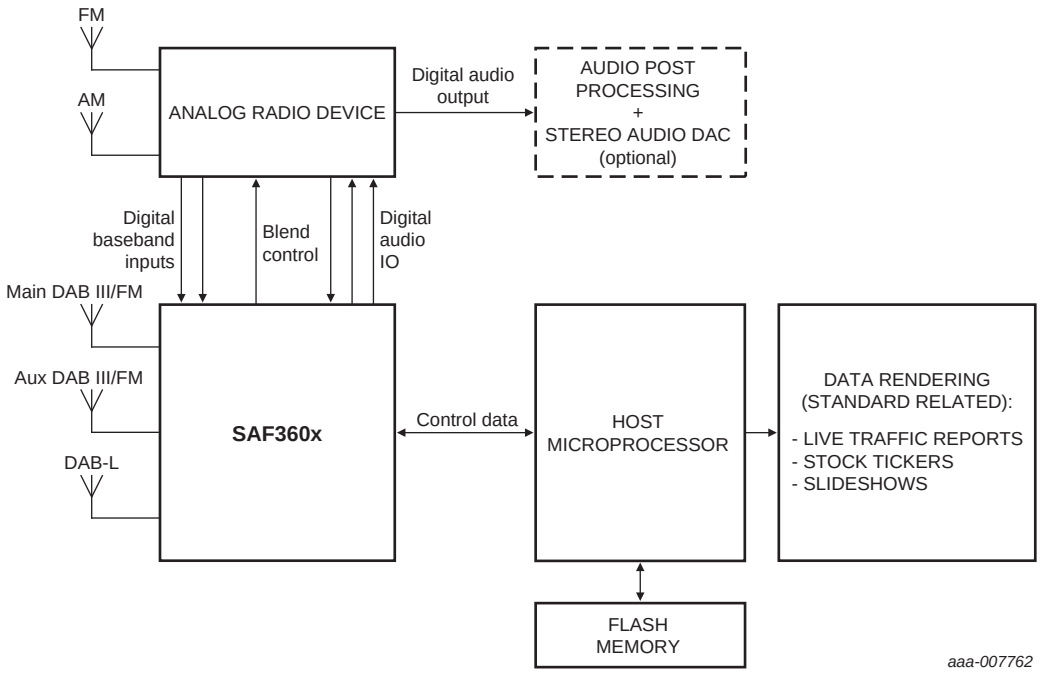


Fig 3. System block diagram – SAF3601, SAF3602, SAF3604, SAF3606

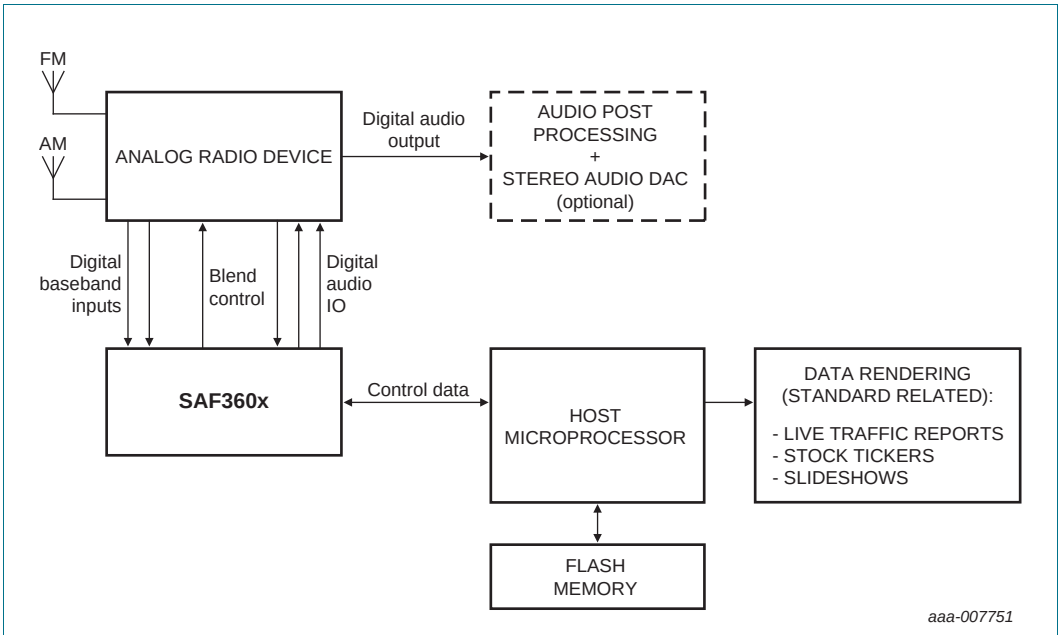


Fig 4. System block diagram – SAF3600, SAF3607

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
SAF3601, SAF3602, SAF3604, SAF3606					
$V_{DDA(VREG)(3V3)}$	voltage regulator analog supply voltage (3.3 V)		–0.5	+3.9	V
VREG_CONTROL	1.8 V external supply control/status		–0.5	+1.89	V
VREG_SENSE	external sense pin		–0.5	+1.89	V
$V_{DDA(ADPLL1)(1V8)}$	ADPLL1 analog supply voltage		–0.5	+1.89	V
$V_{DDA(XTAL)(1V8)}$	crystal analog supply voltage		–0.5	+1.89	V
$V_{DDA(DCO1)(1V8)}$	DCO1 analog supply voltage		–0.5	+1.89	V
$V_{DDA(DIV)(1V8)}$	DIV analog supply voltage		–0.5	+1.89	V
$V_{DDA(LVHFA)(1V8)}$	LVHFA analog supply voltage		–0.5	+1.89	V
$V_{DDA(VHFM)(1V8)}$	VHFM analog supply voltage		–0.5	+1.89	V
$V_{DDA(DCO2)(1V8)}$	DCO2 analog supply voltage		–0.5	+1.89	V
$V_{DDA(ADPLL2)(1V8)}$	ADPLL2 analog supply voltage		–0.5	+1.89	V
$V_{DDA(ADC)(1V8)}$	ADC analog supply voltage		–0.5	+1.89	V
$V_{DDD(ADPLL1)(1V8)}$	ADPLL1 digital supply voltage		–0.5	+1.89	V
$V_{DDD(ADPLL2)(1V8)}$	ADPLL2 digital supply voltage		–0.5	+1.89	V
$V_{DDD(RFE)(1V8)}$	RFE digital supply voltage		–0.5	+1.89	V
$V_{DD(IO)}$	input/output supply voltage		–0.5	+3.9	V
V_{QPS}	OTP programming voltage (2.5 V)		–0.5	+3.0	V
$V_{DD(A)}$	analog blocks supply voltage		–0.5	+1.7	V
$V_{DD(C)}$	core supply voltage		–0.5	+1.7	V
SAF3600, SAF3607					
$V_{DD(IO)}$	input/output supply voltage		–0.5	+3.9	V
V_{QPS}	OTP programming voltage (2.5 V)		–0.5	+3.0	V
$V_{DD(A)}$	analog blocks supply voltage		–0.5	+1.7	V
$V_{DD(C)}$	core supply voltage		–0.5	+1.7	V
Input voltages/current					
V_i	input voltage		–0.5	$+V_{DD(IO)}$	V
$V_{i(VHF)(diff)}$	peak differential VHF input voltage	between pins VHF_MAIN_IN_P and VHF_MAIN_IN_N or pins VHF_AUX_IN_P and VHF_AUX_IN_N; AC coupling	-	+1.7	V
$V_{i(L\text{-}band)}$	peak L-band input voltage	pin LBAND_IN; AC coupling	-	+1.7	V

Table 4. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	human body model	[1]	−1500	+1500	V
		charged device model				
		corner pins	[2]	−750	+750	V
		other pins	[3]	−400	+500	V
I_{lu}	latch-up current		[4]	−10	+10	mA
Temperature						
T_{amb}	ambient temperature			−40	+85	°C
T_{stg}	storage temperature			−65	+150	°C

[1] In accordance with *AEC-Q100-002 H1C*.

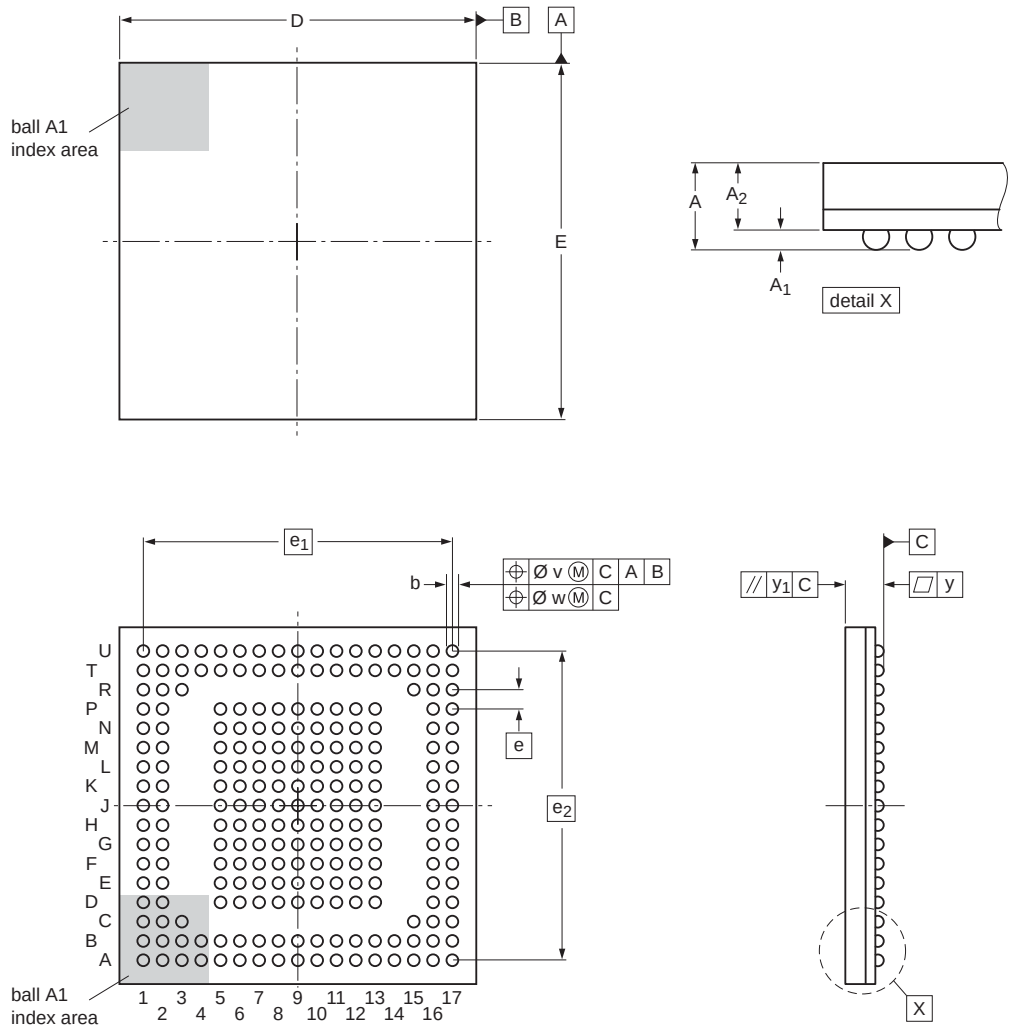
[2] In accordance with *AEC-Q100-011 C3A*.

[3] In accordance with *AEC-Q100-011 C2*.

[4] All supply voltages below the maximum values listed in this table.

8. Package outline

LFBGA223: plastic low profile fine-pitch ball grid array package; 223 balls **SOT1322-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
	max	1.45	0.35	1.10	0.45	12.1	12.1							
mm	nom	1.30	0.30	1.00	0.40	12.0	12.0	0.65	10.4	10.4	0.15	0.08	0.1	0.1
	min	1.20	0.25	0.95	0.35	11.9	11.9							

sot1322-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1322-1		MO-205				~~12-01-02~~ 12-01-23

Fig 5. Package outline SOT1322-1 (LFBGA223)

9. Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAF360X_FAM_SDS v.2	20140822	Product short data sheet	-	SAF360X_FAM_SDS v.1
Modifications	• Updated data sheet with SAF3601, SAF3602, SAF3604 and SAF3606 variants			
SAF360X_FAM_SDS v.1	20140716	Product short data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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ICs with DAB, DAB+ or T-DMB functionality

Use of this product in any manner that complies with the DAB, DAB+ or T-DMB digital radio standards requires a license under applicable patents in the DAB patent portfolio covering mainly the two technologies COFDM radio reception and MPEG audio layer II decoding, which license must be obtained from Koninklijke Philips Electronics N.V. via Philips Intellectual Property and Standards (www.ip.philips.com), e-mail: info.licensing@philips.com.

ICs with MPEG-2 AAC, MPEG-4 AAC or MPEG-4 BSAC functionality

Use of this product in any manner that complies with the MPEG-2 AAC, MPEG-4 AAC or MPEG-4 BSAC audio compression standards requires a license under applicable patents in the MPEG-2 AAC and MPEG-4 AAC patent portfolio, which license is available from Via Licensing Corporation, 1000 Brannan street, Suite 200, San Francisco, CA 94103.

ICs with T-DMB functionality

Use of this product in any manner that complies with the T-DMB standard, which includes an MPEG-2 transport stream, is expressly prohibited without a license under applicable patents in the MPEG-2 patent portfolio, which license is available from MPEG-LA, L.L.C., 250 Steele Street, Suite 300, Denver, Colorado 80206.

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11. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

12. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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